REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The non-Final Office Action of November 18, 2002 has been received and contents carefully reviewed.

Claims 1-20 are currently pending. Claims 6-20 are withdrawn from consideration as being drawn to a non-elected invention. Claim 1 has been amended. Reexamination and reconsideration are respectfully requested.

The Examiner objected to the drawings because of inconsistencies between the reference number in the drawings and the reference numbers in the specification. Applicants have amended the specification to correct these minor informalities in Figures 3D, 3E, and 4. Applicants submit a Transmittal of Drawing Correction herewith to correct the informalities in Figure 5. No new matter has been added. Applicants request that the objections be withdrawn.

The Examiner rejected claims 1 and 2 under 35 USC 102(e) as being anticipated by Applicant's Figures 1-4; and rejected claims 1 and 2 as being anticipated by Song et al. (US Patent No. 6,163,356). Applicants respectfully traverse these rejections.

Claim 1 is allowable at least for the reason that claim recites a combination of elements including a gate pad electrode at one end of the gate line; wherein the gate pad electrode is formed directly on top of the first insulating layer, wherein the first insulating layer includes an opening that exposes a portion of the gate line, and wherein the gate pad electrode electrically contacts the exposed portion of the gate line and overlaps the first insulating layer. None of the cited references teaches or suggests each and every feature of the claims.

Neither Applicants Figures nor Song et al. disclose a gate pad electrode directly on the top of a first insulating layer and wherein the gate pad electrode electrically contacts the exposed portion of the gate line and overlaps the first insulating layer as in claim 1.

Moreover, claims 2-5 are allowable by virtue of their dependence on claim 1, which is believed to be allowable.

Claims 3-5 are objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Applicants believe the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7371.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

Dated: February 5, 2003

Respectfully submitted,

By _____
Teresa M. Arroyo
Registration No.: 50,015
MCKENNA LONG & ALDRIDGE LLP
1900 K Street, N.W.
Washington, DC 20006
Telephone: (202) 496-7500
Facsimile: (202) 496-7756
Attorneys for Applicant

Version With Markings to Show Changes Made

In the Specification

Please amend the specification as follows:

On page 3, paragraph beginning on line 20:

Still referring to Figure 2, gate and data pads 21 and 23 are integrally formed as terminal portions of the gate and data lines 22 and 24, respectively. Over the gate and data pads 21 and 23 area gate pad electrode 34 and a data pad electrode 36. The gate and data pads 21 and 23 are electrically connected with the gate pad electrode 34 and the data pad electrode 36 via a gate pad contact hole [42] 44 and a data pad contact hole [44] 42, respectively. The gate pad electrode 34 and the data pad electrode 36 are electrically connected with external driving circuits (not shown) that drive the TFT "S" and the pixel electrode 14.

On page 6, paragraph beginning on line 15:

Next, as shown in Figure 3D, an insulating layer is deposited and patterned using a fourth mask to form a passivation layer 56, which serves to protect the active layer 55. The passivation layer 56 is either an inorganic material such as silicon oxide (SiO_2), or an organic material such as benzocyclobutene (BCB). Those materials have high light-transmittance, good humidity resistance, and good reliability, all of which are required. In addition, a data pad contact hole [40] 42, a drain contact hole 32, and a storage contact hole [42] 40 are formed through the passivation layer 56 to [respectively] expose portions of the second storage electrode 58, the drain electrode 30, and the data pad 23. The drain contact hole 32 and the storage contact hole 40 respectively serve to electrically connect the drain electrode 30 and second storage electrode 58 to a pixel electrode 14 (see Figure 2 and Figure 3E). Further, the data pad contact hole 42 serves to electrically connect the data line 24 with a data pad electrode 36 (also see Figure 2 and Figure 3E).

On page 7, paragraph beginning on line 22:

Figure 4 is a cross-sectional view taken along a line "IV-IV" of Figure 2. As shown, a gate pad 21 electrically contacts a gate pad electrode 34. First, a gate pad 21 is formed on the substrate 1. Then, a gate insulating layer 50, an amorphous silicon layer 57, and a passivation layer 56 are sequentially formed over the substrate 1. When the drain contact hole (reference 32 of Figures 2 and 3D) is patterned through the passivation layer 56, a gate pad contact hole 44 is formed through the gate insulating layer 50, the amorphous silicon layer 57, and the passivation layer 56. Therefore, a portion of the gate pad 21 is exposed by the gate pad contact hole 44. When a gate pad electrode 34 is formed over the gate pad 21, they are electrically connected to each other via the data pad contact hole [44] 42.

On page 13, paragraph beginning on line 14:

Next, as shown in Figure 6C, using the passivation layer 112 as a mask, the exposed doped amorphous silicon layer 154 is etched away. The exposed portions of the drain electrode 116 and data pad 120 are also etched away such that the drain contact hole [122] 117 and the data pad contact hole [117] 122 are formed. Since the drain electrode 116 and the data pad 120 are comprised of a metal that can be dry-etched it is possible to etch both the metal and the doped amorphous silicon layer 152 together. The drain contact hole [122] 117 and the data pad contact hole [122] 117 expose inner side portions of the drain electrode 116 and the data pad 120, and planar portions of the gate insulating layer 150.

In the Claims

Please amend the claims as follows:

1. A liquid crystal display device comprising:

a substrate;

a thin film transistor including a gate electrode, a source electrode, and a drain electrode on the substrate;

a pixel electrode electrically connected to the drain electrode;

a data line electrically connected with the source electrode;

a first insulating layer, a pure amorphous silicon layer, and a doped amorphous silicon layer sequentially layered under the data line; a data pad at one end of the data line; a gate line electrically connected with the gate electrode; and

a gate pad electrode at one end of the gate line;

wherein the gate pad electrode is formed directly on top of the first insulating layer, wherein the first insulating layer includes an opening that exposes a portion of the gate line, and wherein the gate pad electrode electrically contacts the exposed portion of the gate line and overlaps the first insulating layer.